WHAT IS CLAIMED IS:

1. An integrated module comprising:

a circuit;

a plurality of input/output terminals, each connected to a driver circuit for driving output signals and to a reception circuit for receiving input signals;

a first delay element with a first delay time, wherein the first delay element is capable of being connected into or disconnected from a signal path of a circuit-internal signal, in order to delay or to accelerate the circuit-internal signal, respectively;

a first test delay element at a first input/output terminal pair, wherein the first test delay element is constructed in a substantially similar manner to the first delay element; and

a test control unit configured to, in a test operation, to determine the first delay time by means of a signal propogation time beween the two input/output terminals of the first input/output terminal pair.

2. The integrated module of claim 1, comprising:

a second delay element with a second delay time different from the first delay time, wherein the first and second delay elements are capable of being connected into or disconnected from the signal path of the circuit-internal signal separately, in order to delay or to accelerate the circuit-internal signal.

3. The integrated module of claim 2, comprising a second test delay element at a second input/output terminal pair, wherein the second test delay element is constructed in a substantially similar manner to the second delay element; and

the test control unit is configured to, in a test operation, determine the second delay time by means of a signal propogation time beween the two input/output terminals of the second input/output terminal pair.

4. The integrated module of claim 3, comprising:

a delay control unit coupled with the first and second delay elements in order to delay or accelerate the signal by connection or disconnection of the first and/or the second delay elements to the signal path; and

a non-volatile setting memory in order to store a setting value which determines the connection and the disconnection of the delay elements by the delay control unit.

5. The integrated module of claim 3, wherein the two input/output terminals of the first and the second input/output terminal pair are arranged adjacent to one another.

6. The integrated module of claim 3, wherein the first and/or the second test delay element can be switched on and off in accordance with the test control unit, in order to connect the first and/or the second test delay element to the respective input/output terminal pair only during the test operation.

7. The integrated module of claim 1, wherein the driver circuit and the reception circuit of each of the input/output terminals can be switched on/off in accordance with the test operation.

8. A method for setting a temporal position of a signal in a signal path of a circuit of an integrated module to a desired signal position, comprising:

in a test operation, measuring a delay time of a first delay element in a signal path of an in-circuit signal by propagating a singal through a first test delay element whose structure is substantially similar to the first delay element; and

selectively connecting or disconnecting the first delay element to the signal path based on results of measuring the delay time of the first delay element.

9. The method of claim 8, further comprising:

in a test operation, measuring a delay time of a second delay element in the signal path of the in-circuit signal by propagating a singal through a second test

delay element whose structure is substantially similar to the second delay element; and

selectively connecting or disconnecting the second delay element to the signal path based on results of the measuring the delay time of the second delay element

10. The method of claim 8, wherein the switching-on/off of the first and/or the second delay element is carried out in such a way that the total delay time due to the first and/or the second delay element is set in accordance with the measured first and second delay time such that the signal position of the signal corresponds as precisely as possible to the desired signal position.

11. The method of claim 10, further comprising storing the setting determined with regard to the switching-on/off of the first and/or the second delay element in non-volatile storage in the integrated module, allowing the temporal position of the signal to be retained.

12. The method of claim 11, wherein storing the setting determined with regard to the switching-on/off of the first and/or the second delay element in non-volatile storage in the integrated module comprises modifying the state of fuses.

13. The method of claim 8, wherein the test operation is performed during a manufacturing process.

14. A dynamic random access memory (DRAM) device, comprising:

one or more memory elements controlled by signals having associated setup and hold times;

a plurality of input/output terminals, each connected to a driver circuit for driving output signals and to a reception circuit for receiving input signals;

a plurality of delay elements with corresponding delay times, each capable of being connected into or disconnected from a signal path carrying one of the control signals, in order to delay or to accelerate the one control signal, respectively;

a plurality of delay elements, each constructed in a substantially similar manner to one of the delay elements; and

a test control unit configured to, in a test operation, to determine delay times of the delay elements by means of a signal propogation times beween the input/output terminals of the input/output terminal pairs.

15. The DRAM of claim 14, further comprising a delay control unit to selectively connect or disconnect the delay elements to the signal path based on the delay times determined by the test control unit.

16. The DRAM of claim 15, further comprising a plurality of non-volatile storage elements to store settings indicating, to the delay control unit, which delay elements should be connected or disconnected to the signal path.

17. The DRAM of claim 16, wherein the non-volatile storage elements are set during a manufacturing process.